WIMNACT WS & IEEE EDS Mini-colloquim on Nano-CMOS Technology
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CMOS Scaling and Variability

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NEC

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Acknowledgements

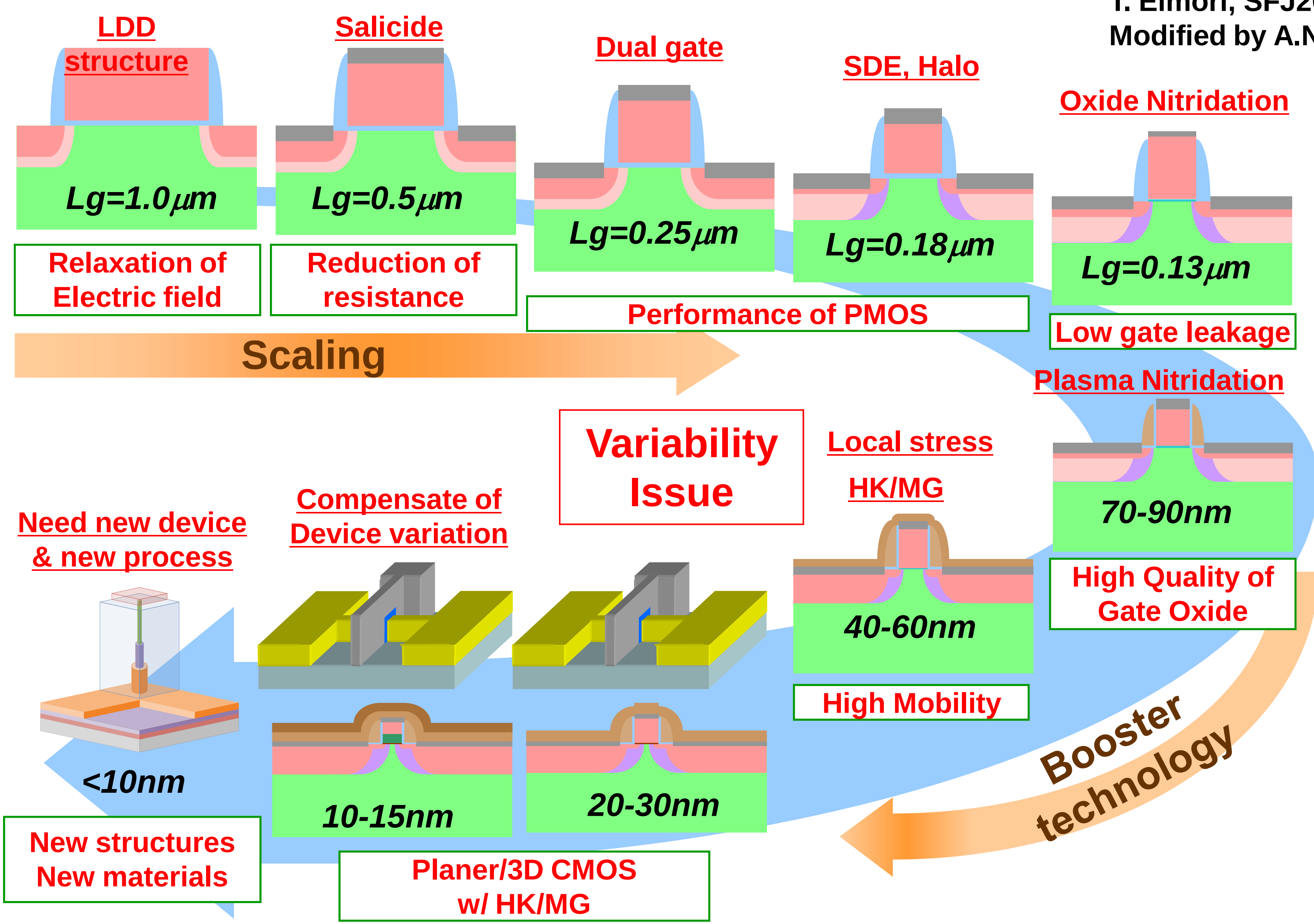
- I would like to thank members of Robust program in MIRAI project for supporting data, and especially Dr. A. Nishida for discussing a lot of issues.
- This work is supported by NEDO.

Outline

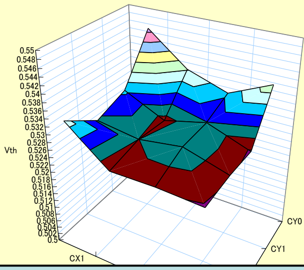
1. CMOS scaling and Variation
2. Evaluation methods of Variation
3. How to improve variation?
4. Summary

CMOS scaling and Breakthrough technologies

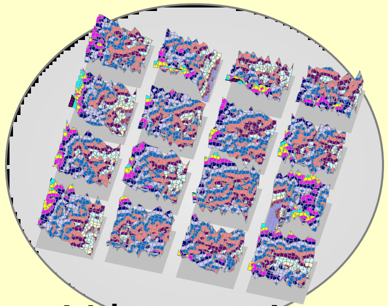
T. Eimori, SFJ2006
Modified by A.N.



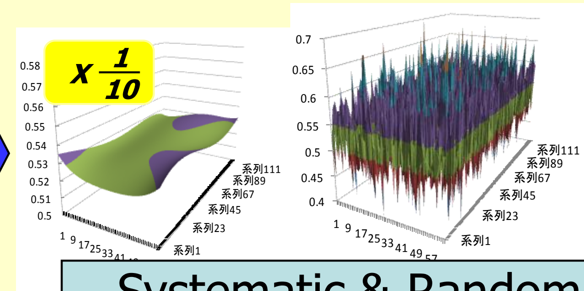
Vth variation on chip and on Wafer



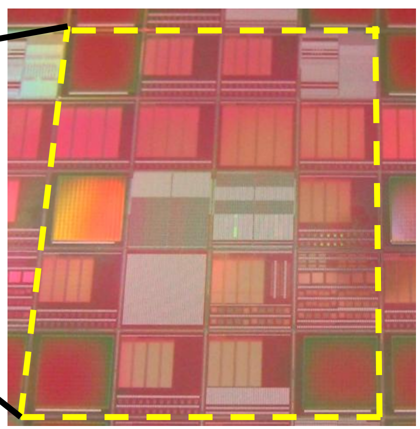
Systematic variation on wafer



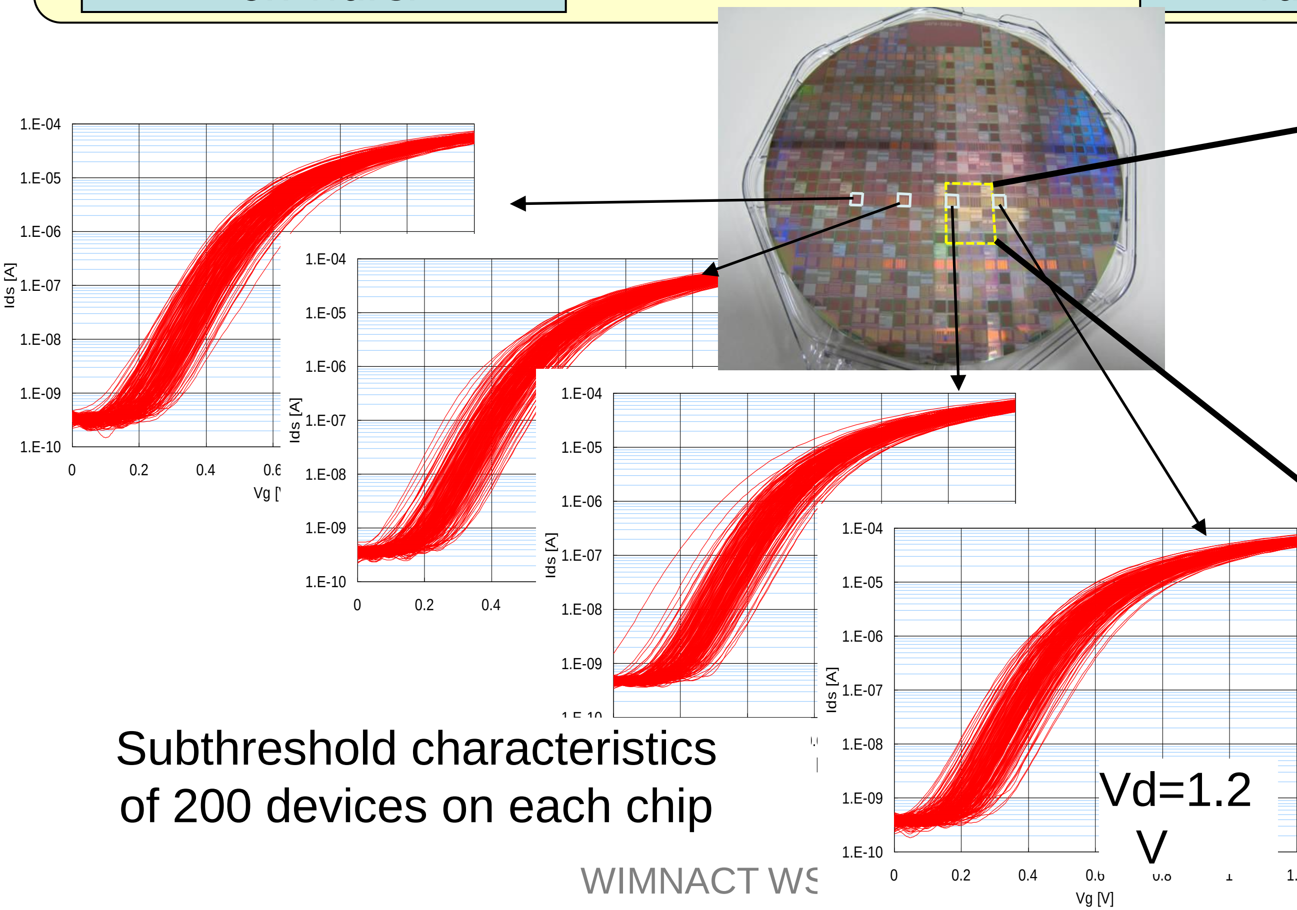
Vth mapping



Systematic & Random variation on chip



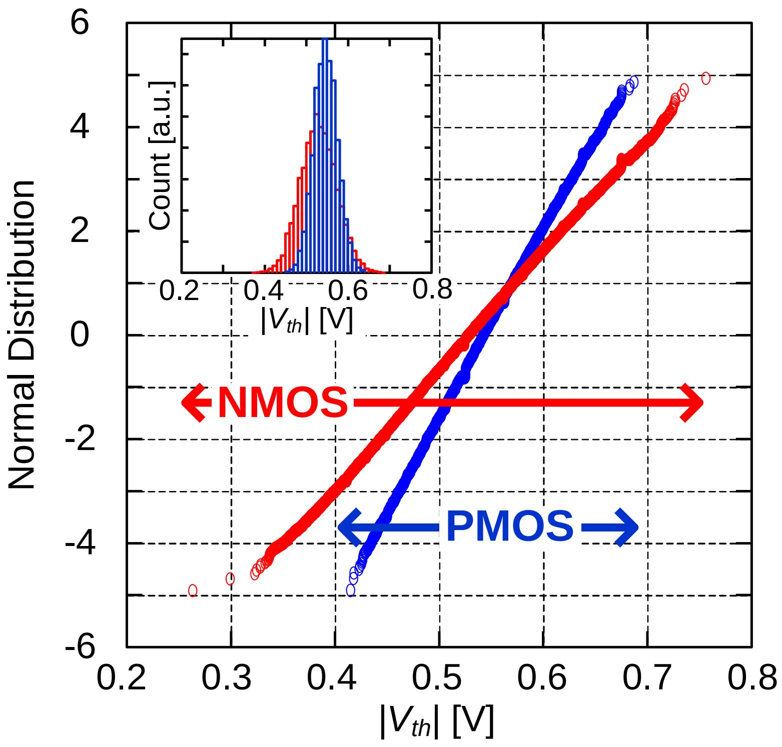
1M DMA-TEG on chip



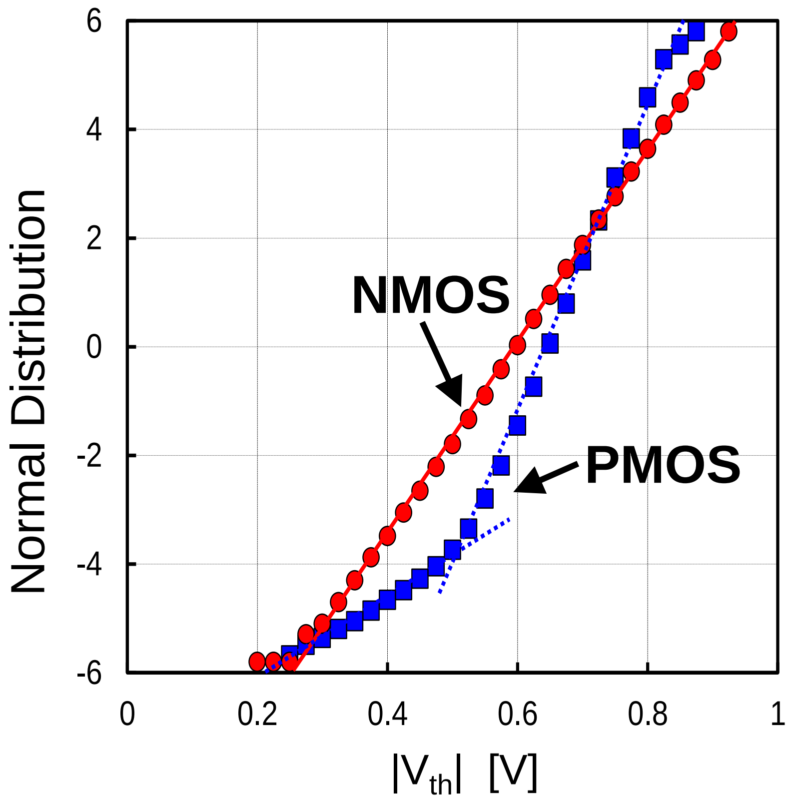
Subthreshold characteristics of 200 devices on each chip

Vth random variation of N/P-FETs

- For 1M devices, Vth variation shows normal distribution.
- For 256M, Vth variation of NFET shows normal, but that of PFET shows normal and tail distribution.



(a) Vth variation for 1M devices



(b) Vth variation for 256M devices

Physical parameter vs. Vth variation

- What is the relationship between physical parameters of MOSFET and Vth variation?
- Theoretical threshold voltage and its standard deviation

Threshold voltage

$$Vt = V_{FB} + \phi_S + \frac{qN_{sub}W_{DEP}}{C_{inv}}$$

Standard deviation

$$\sigma Vt = \frac{q}{C_{inv}}\sqrt{\frac{N_{sub}W_{dep}}{3LW}}$$

- <u>Physical parameter</u>
  - ✓ L : Gate length
  - ✓ W : Gate width
  - ✓ Tox : Gate oxide thickness
  - ✓ Nsub : impurity in Si substrate

  etc.

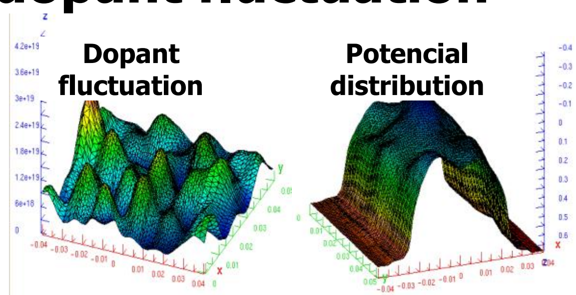
- L, W scaling → Enhance of variation by √(LW).

Variation mechanisms

- Random variation can come from several origins.
- RDF and LER are the main origins of the random variation.

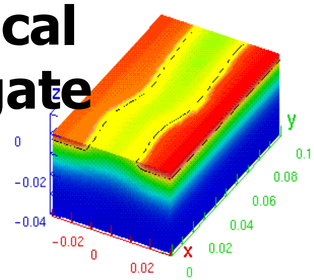
① Random Dopant Fluctuation (RDF)

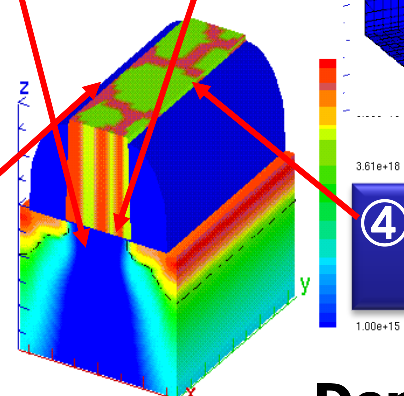
Depend on channel dopant fluctuation



② Line Edge Roughness (LER)

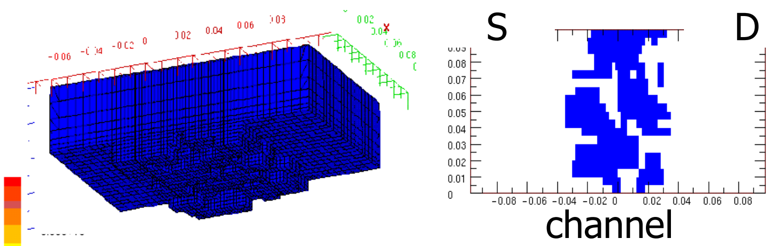
Depend on local variation of gate length





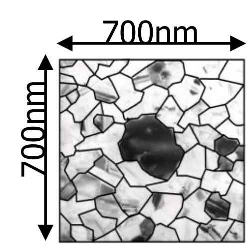
③ Oxide Thickness Fluctuation (OTF)

Depend on gate insulator variation



④ Local grain depletion of gate (LGD)

Depend on local grain-depletion

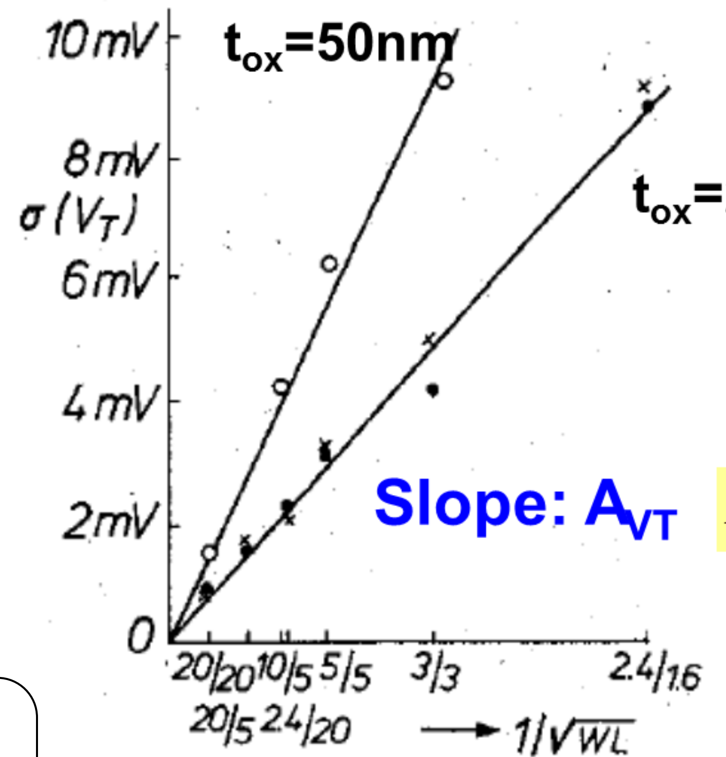


Vth Random Variation & Pelgrom Plot

- Dr. Pelgrom proposed and demonstrated the simple evaluation method of the random variation in 1989.
- This is based on the simple statistics and useful.

$$\sigma_{VTH} = \frac{A_{VT}}{\sqrt{LW}}$$

$$A_{VT} \propto t_{INV}\sqrt{N_{SUB}W_{DEP}}$$



$$\sigma_{VTH} = \frac{A_{VT}}{\sqrt{LW}}$$

$$A_{VT} \propto t_{INV}\sqrt{N_{SUB}W_{DEP}}$$

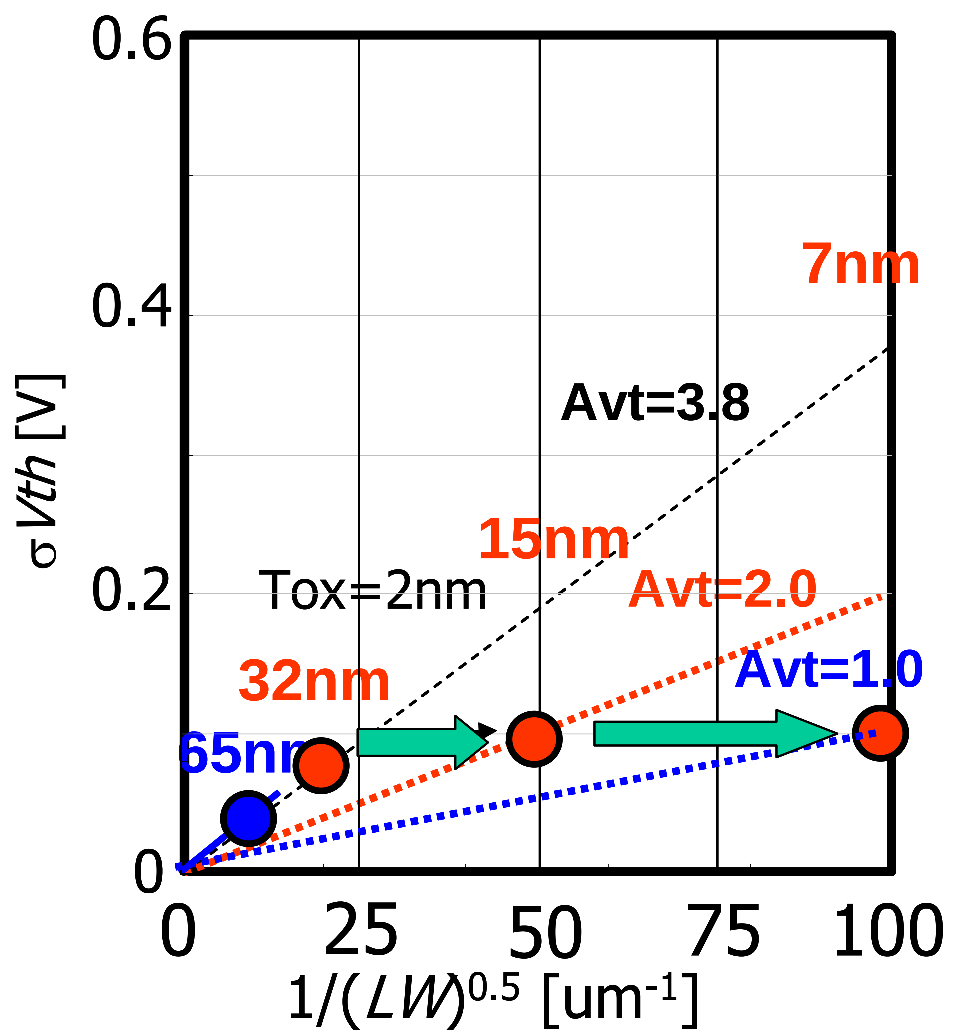
$$\sigma^2 = V\left(\frac{x+y}{2}\right)$$

parameter	n-channel s.d.	p-channel s.d.	unit
A_{VT0}	30	35	mVμm
A_β	2.3	3.2	%μm
A_K	16×10^{-3}	12×10^{-3}	V$^{0.5}\mu$m
S_{VT0}	4	4	μV/μm
S_β	2	2	$10^{-6}/\mu$m
S_K	4	4	10^{-6}V$^{0.5}/\mu$m

M. J. M. Pelgrom et al., IEEE JSSC, vol. 24, p. 1433, 1989.

Vth variation prospect

- Pelgrom plot can foretell the simple prospect of Vth variation.
- Simple device scaling-down can happen large Vth variation.
- If Avt keeps 3.8, 7nm FET will have about 400mV in Vth variation.
- Device parameter optimization, such as Tinv and gate work function, can improve the variation.
- If we need <100mV in Vth variation at 7nm FET, Avt should be 1.0.
- Need the new technology of variation improvement for the future generation.



Outline

1. CMOS scaling and Variation
2. **Evaluation methods of Variation**
3. How to improve variation?
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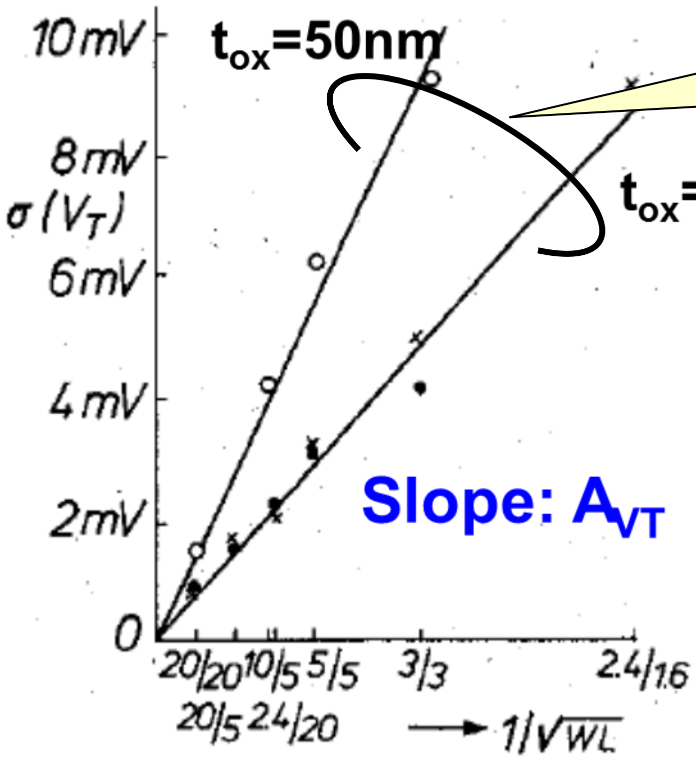
Pelgrom Plot

- Pelgrom plot has been a simple and useful method to evaluate the random variation.
- Is there any issue of Pelgrom plot?

Is variation of 25nm MOSFET really smaller than that of 50nm MOSFET?



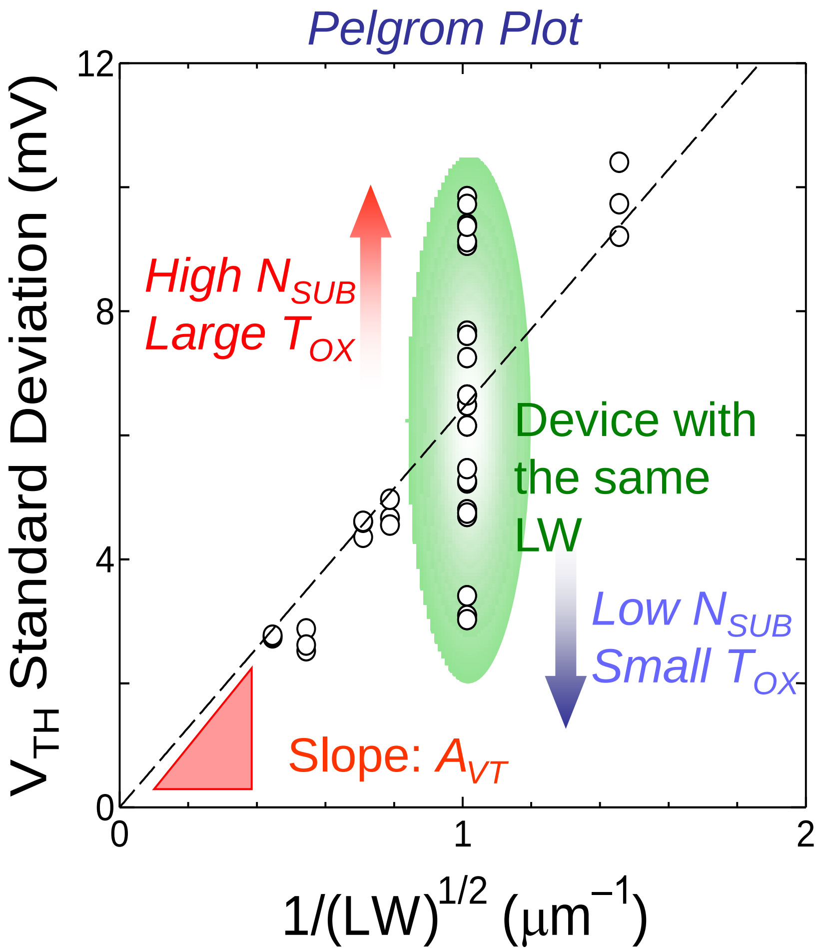
$$\sigma_{VTH} = \frac{A_{VT}}{\sqrt{LW}}$$

$$A_{VT} \propto t_{INV} \sqrt{N_{SUB} W_{DEP}}$$

$$\sigma^2 = V\left(\frac{x+y}{2}\right)$$

Issue of Pelgrom Plot

- Pelgrom plot is very useful when the data come from the devices with the same Tox and Vth. It can make variation date into a straight line.
- However, for the devices with the different Tox and Vth, pelgrom plot cannot make those into a straight line.



K. Takeuchi et al. Silicon Nano. Workshop, p.7, 2007.
K. Takeuchi et al. IEDM, p. 467, 2007.

New normalization method

- New normalization method has been proposed by Dr. K. Takeuchi.
- This can handle the variation data for devices with and w/o different Nsub and Tox.

$$V_{TH} = V_{FB} + 2\phi_F + \frac{qN_{SUB}W_{DEP}}{C_{INV}}$$

$$\frac{qN_{SUB}W_{DEP}}{C_{INV}} = V_{TH} - \left(V_{FB} + 2\phi_F\right) = V_{TH} + 0.1$$

Determined by Impurities

–0.1V for poly-Si gate. It varies in metal gate

$$\sigma_{VTH} = \frac{q}{C_{INV}}\sqrt{\frac{N_{SUB}W_{DEP}}{3LW}}$$

$$= \sqrt{\frac{q}{3\varepsilon_{OX}}}\sqrt{\frac{T_{INV}(V_{TH} - V_{FB} - 2\phi_F)}{LW}}$$

+0.1V

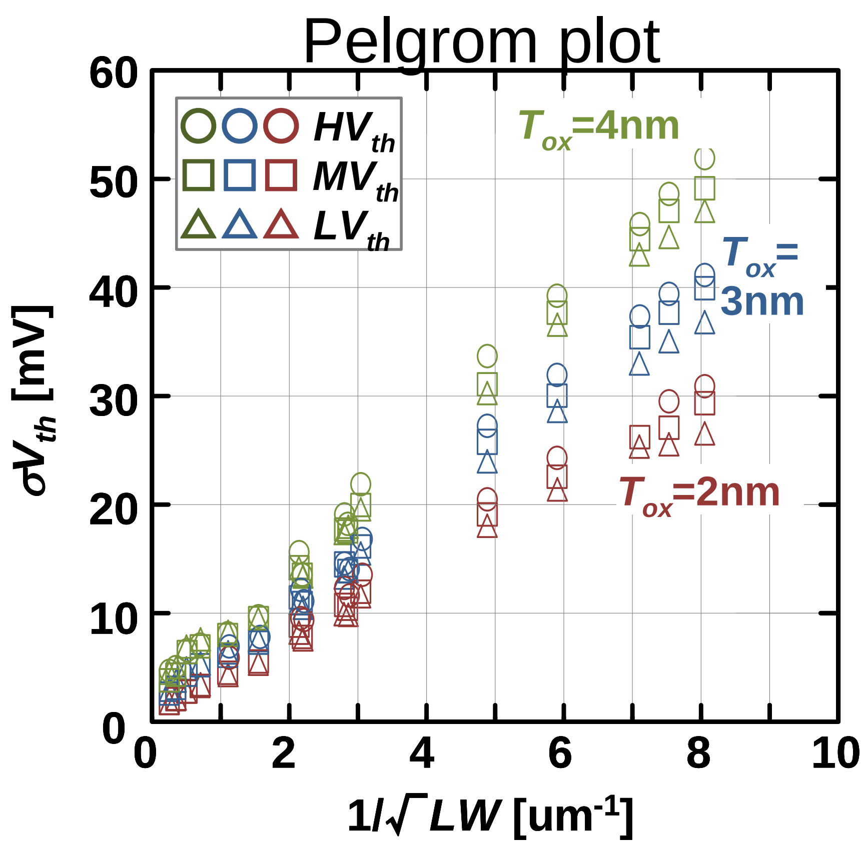
$$\sigma_{VTH} = B_{VT} \times \sqrt{\frac{T_{INV}(V_{TH} - V_{FB} - 2\phi_F)}{LW}}$$

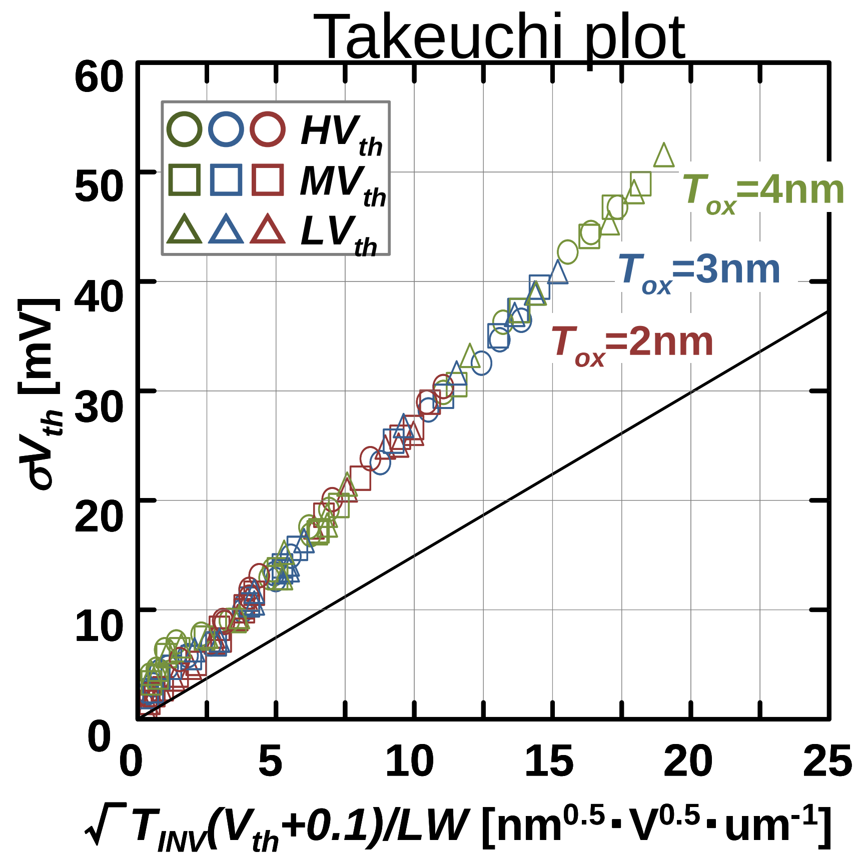
Where, $B_{VT} = \sqrt{\frac{q}{3\varepsilon_{OX}}}$

K. Takeuchi et al. Silicon Nano. Workshop, p.7, 2007.
K. Takeuchi et al. IEDM, p. 467, 2007.

Takeuchi Plot

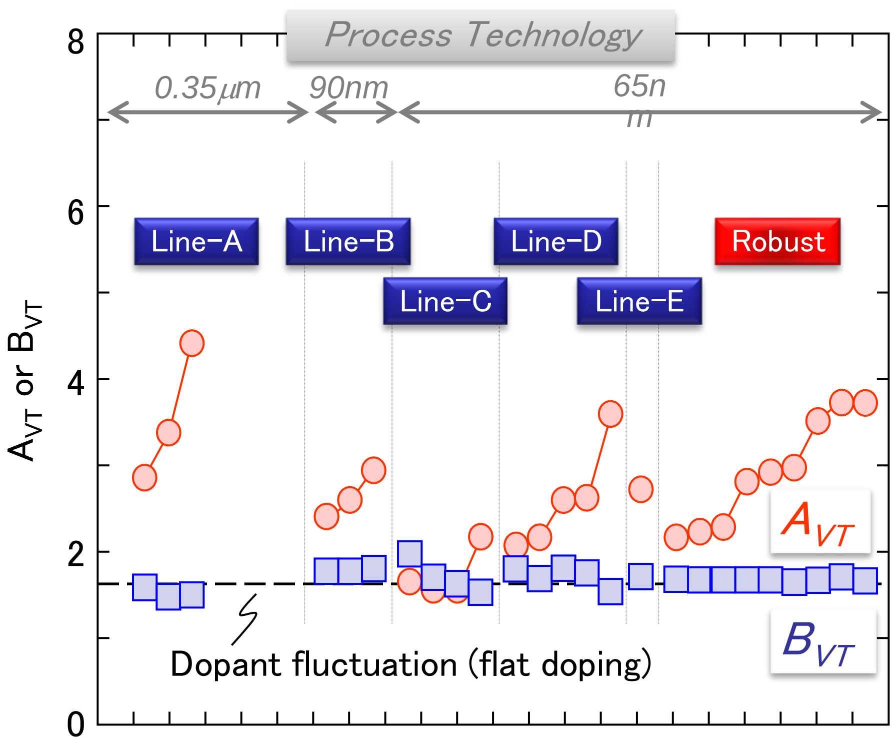
- Pelgrom plot can handle variation data for devices with the same Vth and Tox.
- Takeuchi plot can handle both data and make them into a line if the process is the same.



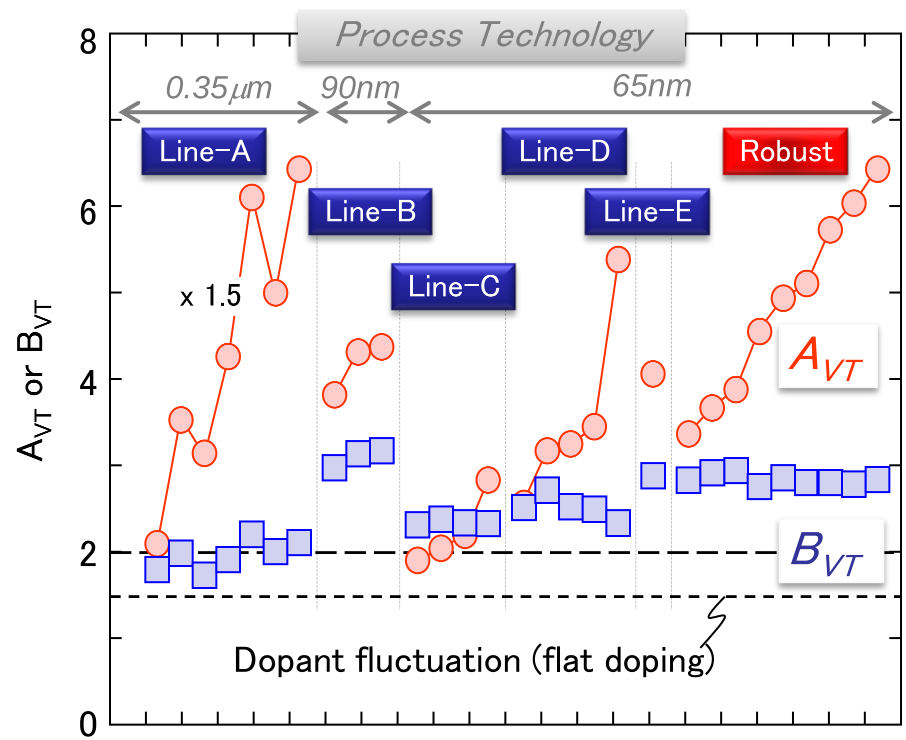


Vth Random Variation

- 0.35um-65nm devices have been analyzed by Takeuchi Plot, which can normalize L, W, Vth, and Tox.
- Vth variation of NFET was larger than that of PFET for every generation.
- PMOS random variation is determined by RDF.
- Origins of NMOS random variation are RDF and others.



P−channel transistors



N−channel transistors

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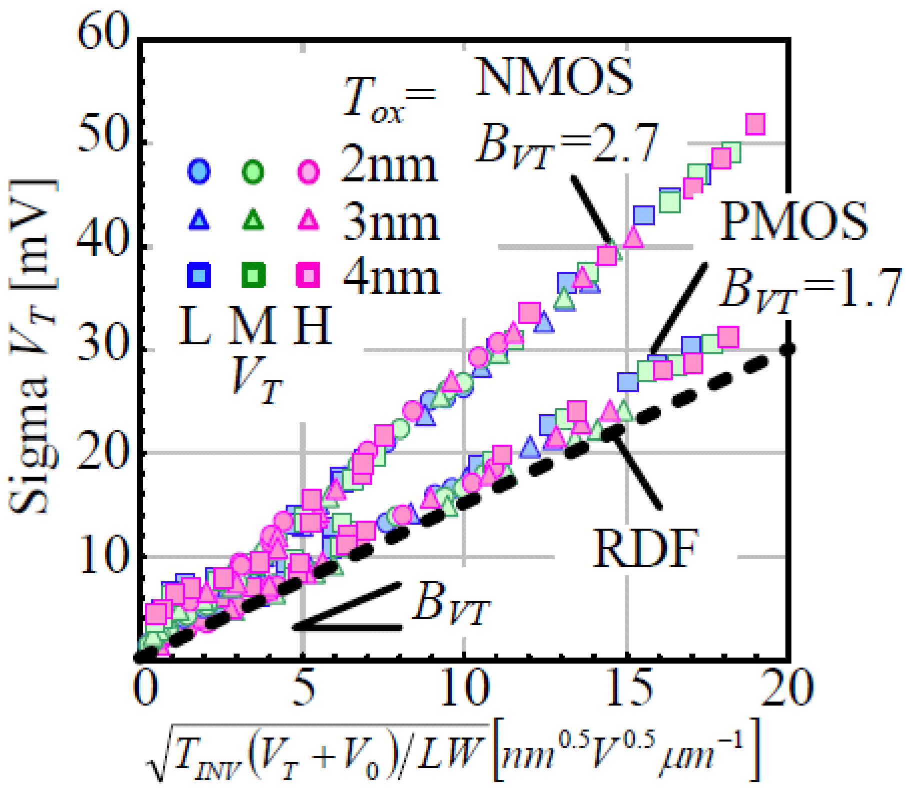
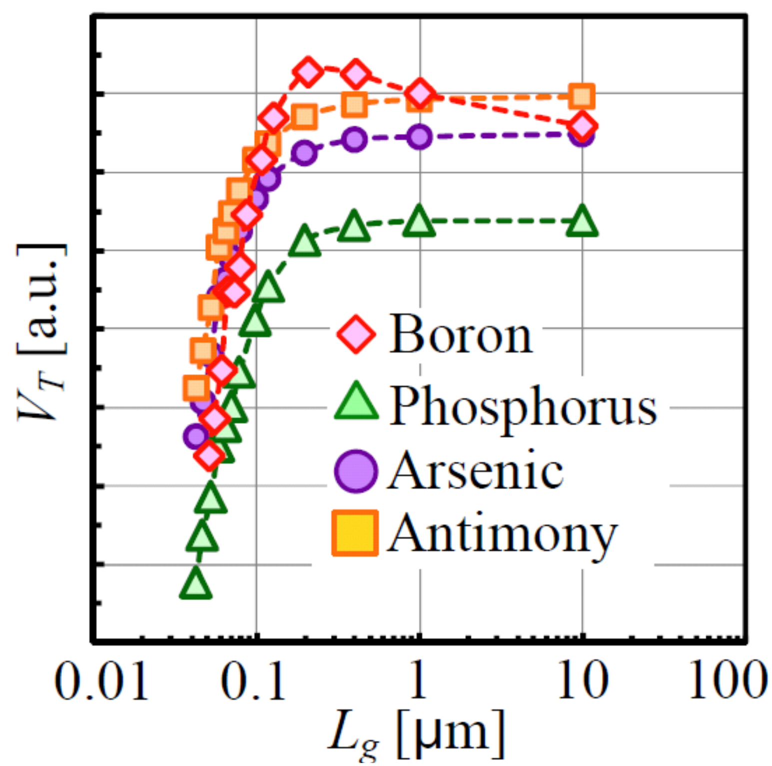
Variation difference

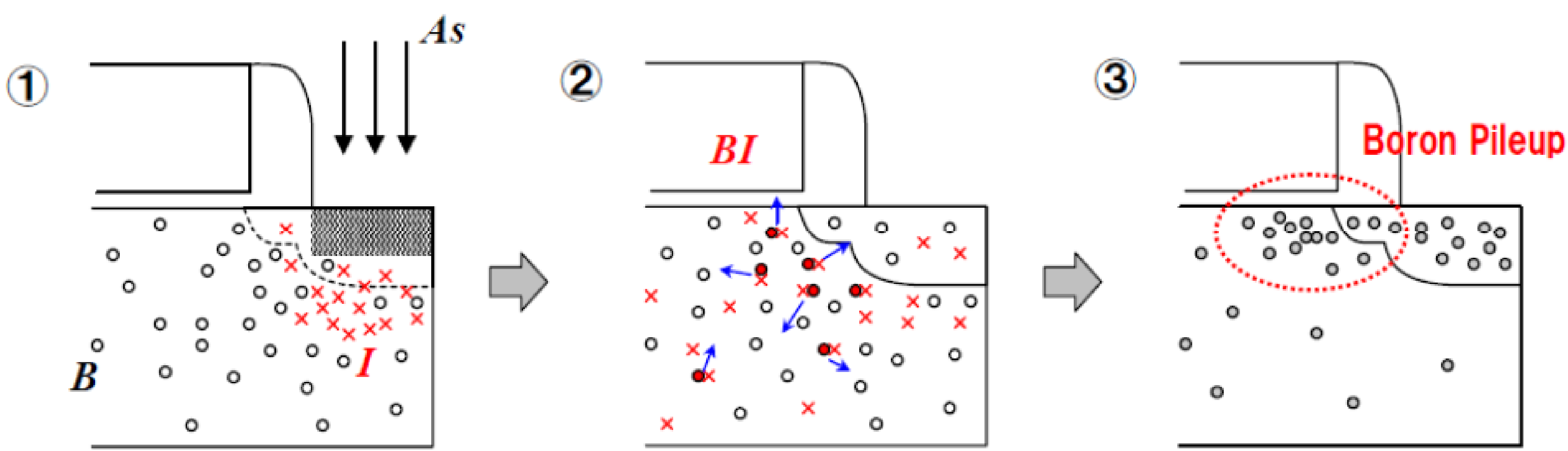
- Takeuchi plot has revealed that Vth variation of NFET was larger than that of PFET for every generation.
- Only NFET with channel Boron showed reverse short channel characteristics. This indicated that channel Boron can be segregated near the junction edge.





Enhanced Variation mechanism

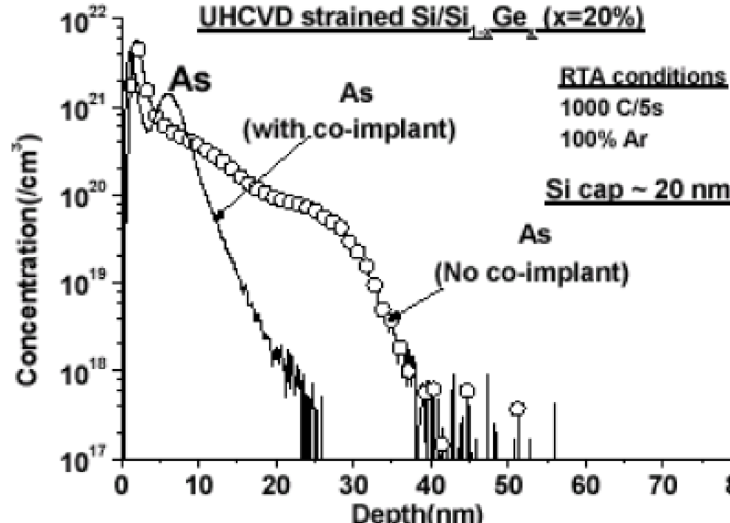
- Boron transient enhanced diffusion (TED) can be the origin of reverse short channel effect and the larger Vth variation of NFET.
- After As I/I for S/D region, interstitial Si (I-Si) has randomly produced near S/D region.
- During S/D annealing, B makes BI complex with I-Si and diffuses in the channel near S/D edges rapidly to happen TED.
- After annealing, B has pileup in the channel region at the edge of the S/D region.
- To control B TED, we need a new technique.



(a) After As I/I (b) During annealing (c) After annealing

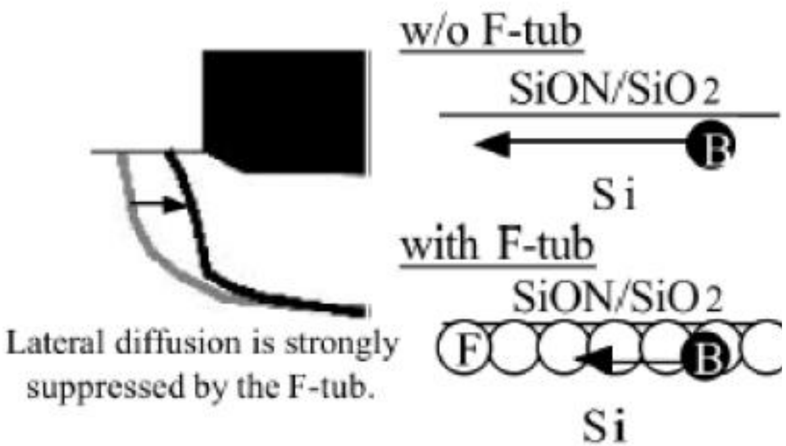
Co-implantation for diffusion control

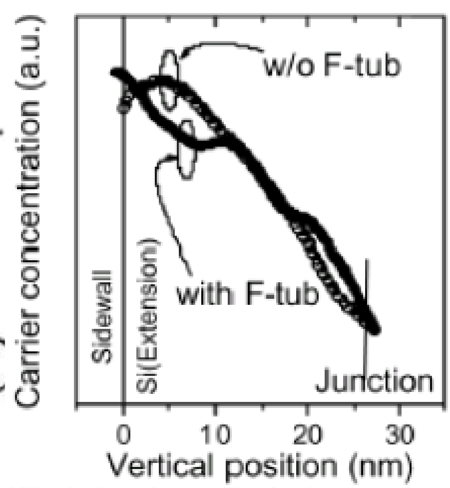
- Co-I/I can suppress dopant diffusion and achieve shallower Xj.
- Better short channel effect and better device characteristics.
- F I/I for PFET: 5E14-2E15

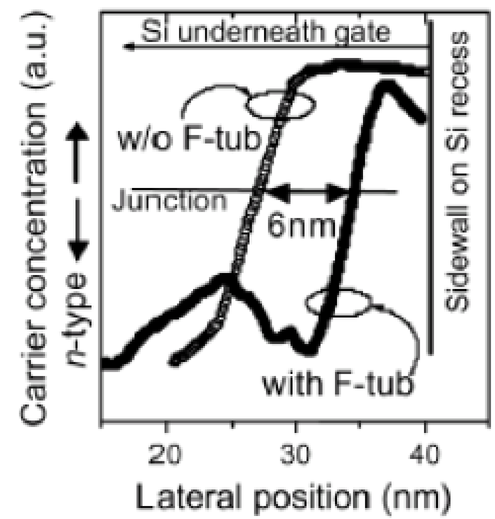


Co-I/I for shallow N+ junction

K.L. Lee et. al., (IBM)IEDM'03





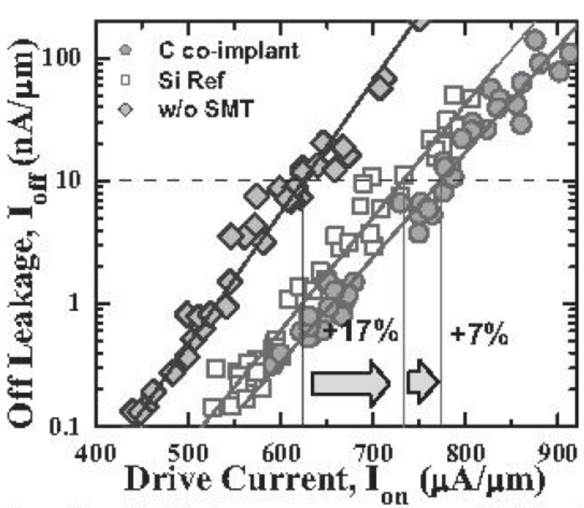


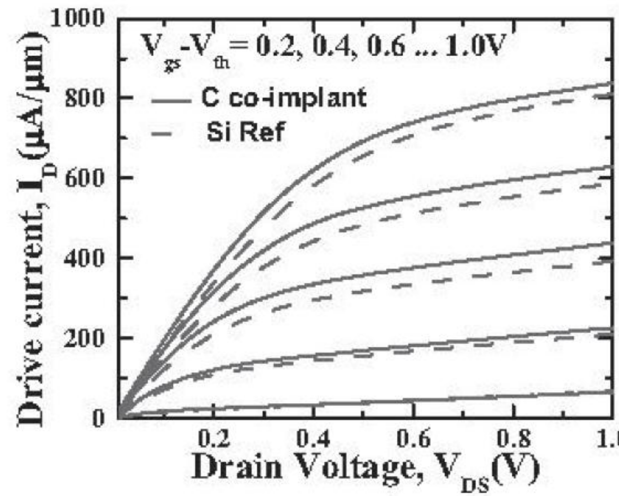
Fluorine co-I/I for shallow P+ junction

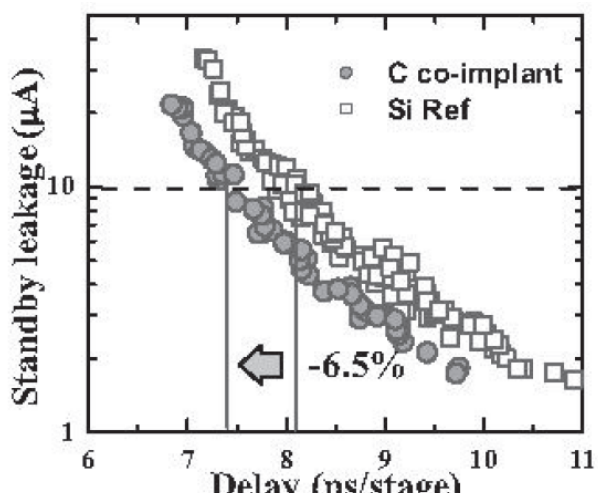
H. Fukutome, et. al., (Fujitsu Lab.)IEDM'03

Carbon co-implantation for diffusion control

- ➢ Carbon co-I/I can control dopant diffusion for NFET.
- ➢ Better short channel effect and on-current by C co-I/I





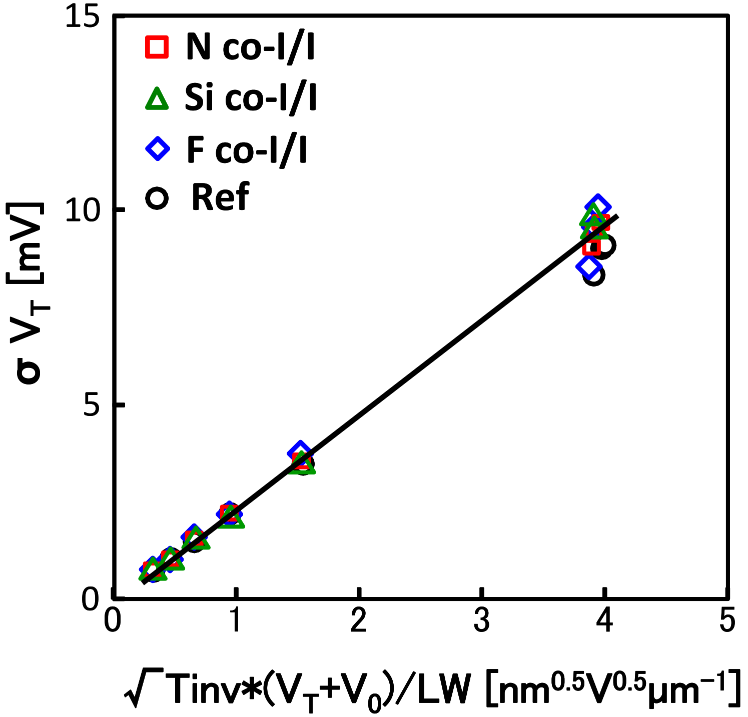


Carbon co-implant	Dose		Energy	
	Low	High	Low	High
Ion Ioff	↔	↔	↔	↔
Overlap Capacitance	↓	↓	↔	↔
Junction Capacitance	↓	↑	↓	↔
GIDL	↓	↑	↓	↑

C.F. Tan et al., VLSI-TSA 2008

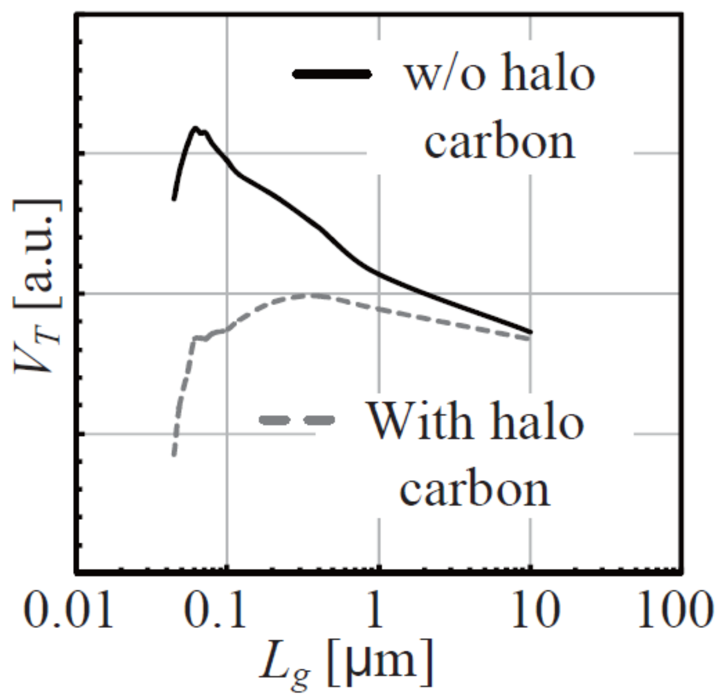
Effect of co-I/I method

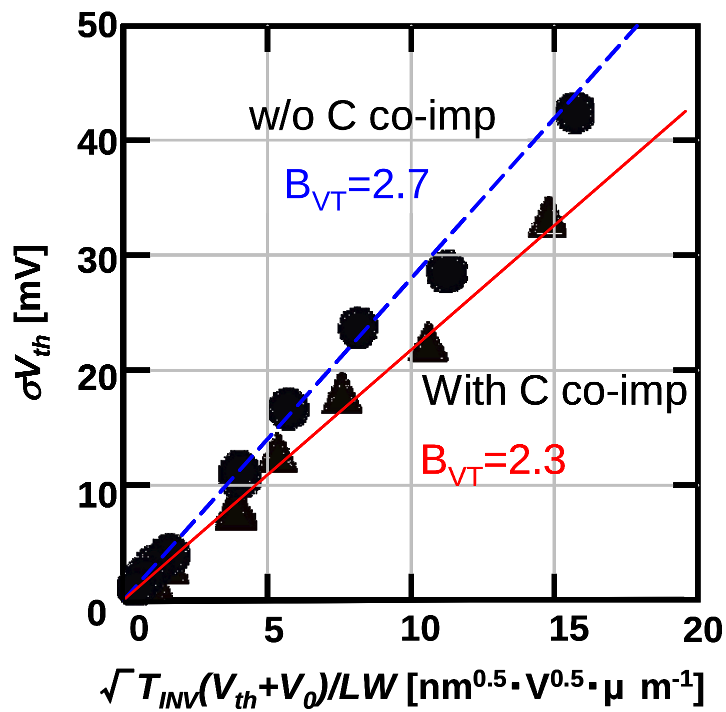
- There are several reports for diffusion control by using Nitrogen, Silicon, Fluorine, and Carbon.
- We have tried co-I/I method to mitigate Vth variation.
- However, co-I/I using Nitrogen, Silicon and Fluorine showed no effect to mitigate Vth variation.



Carbon co-I/I for Variation mitigation

- C co-I/I has improved reverse short channel effect w/o performance degradation for NFET.
- Furthermore, C co-I/I has mitigated Vth variation of NFET.
- This is because Boron TED (Transient Enhanced Diffusion) in channel can be suppressed.

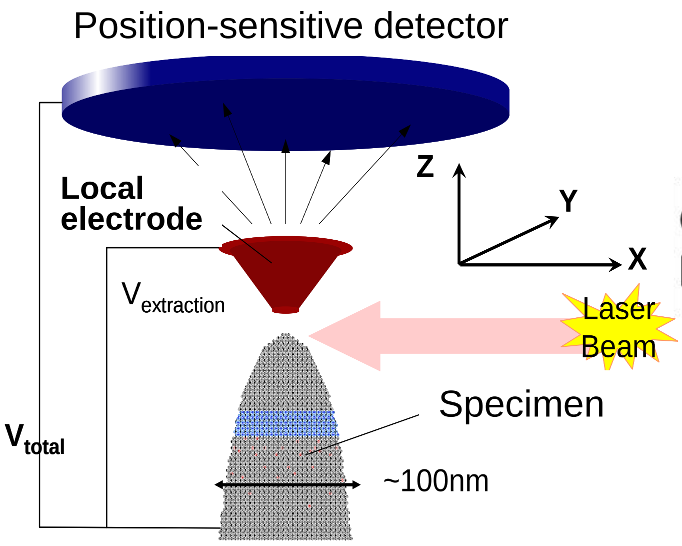




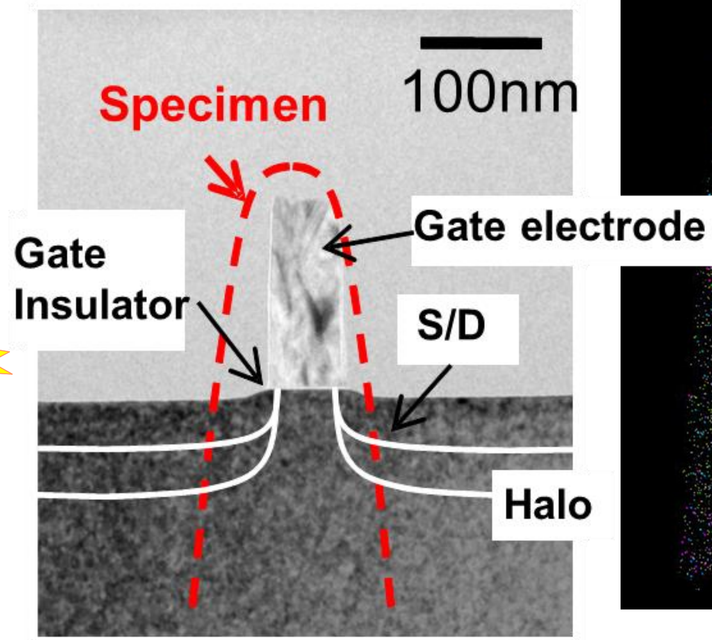
T.Tsunomura et al., VLSI Symp 2009, p.110.

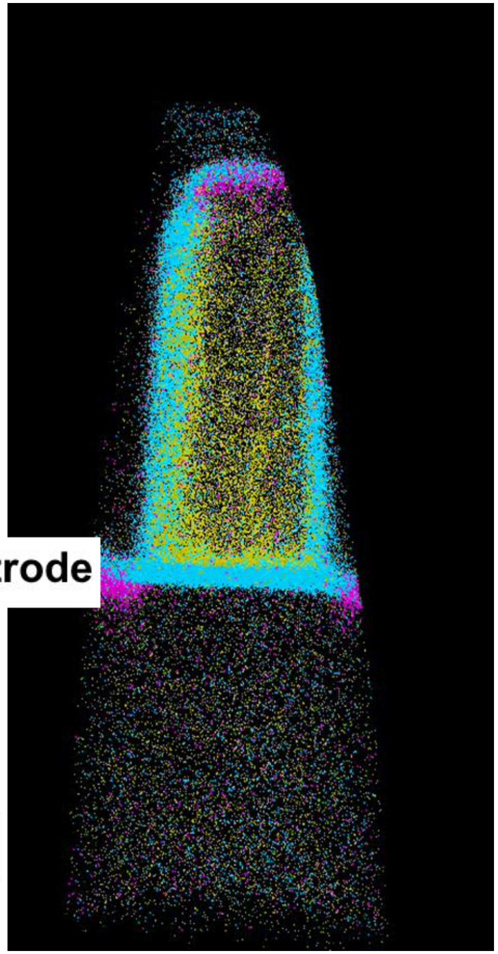
3D Atom Probe Analysis of Si-MOSFET

- 3D Atom probe method can analyze Si-MOSFET structure, including gate insulator.
- RDF in channel can be measured by 3D Atom Probe.



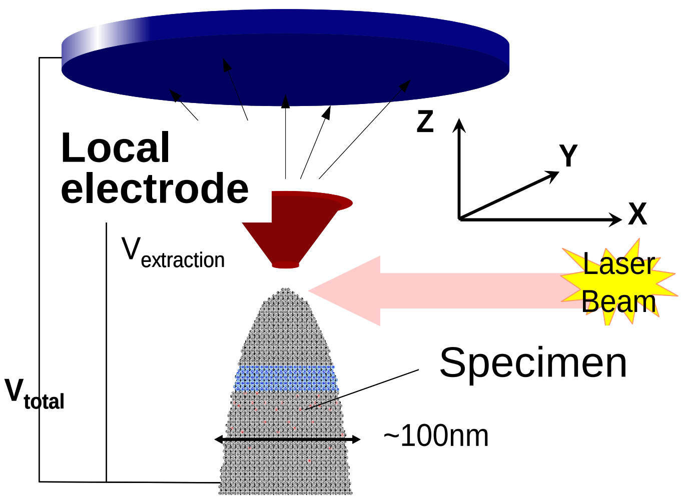
3D Atom Probe System





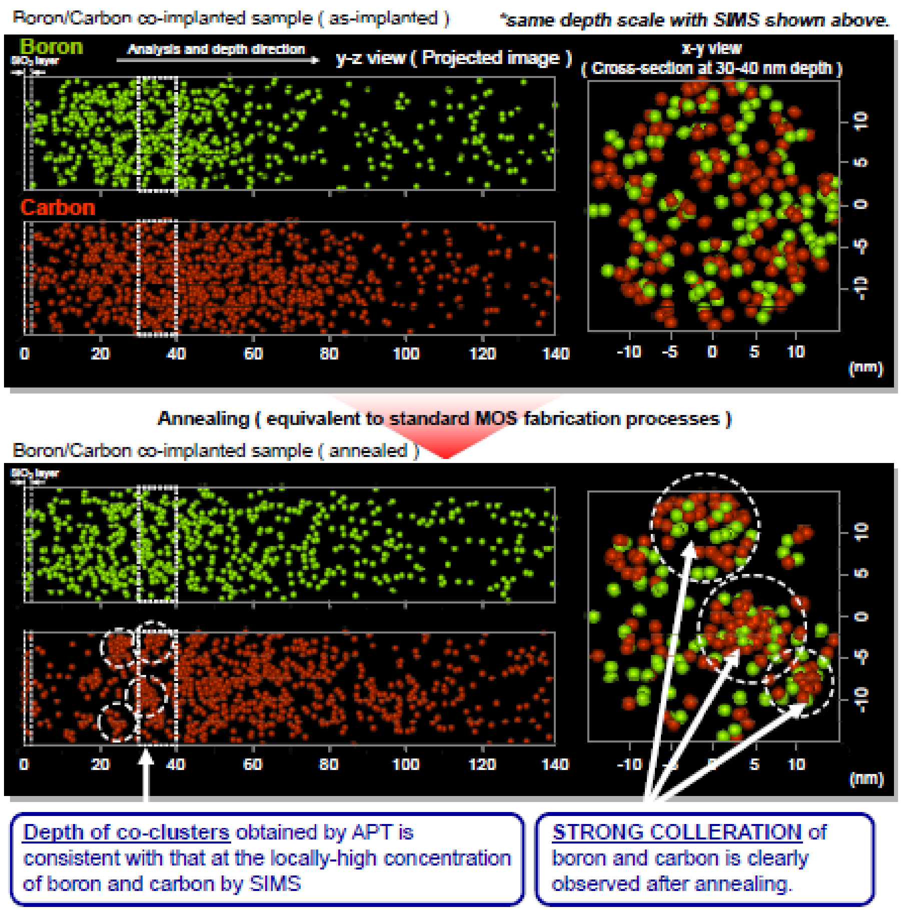
Atom probe analysis of Boron diffusion

- Carbon co-I/I analysis revealed that Boron and carbon co-clusters formed around the projection range of boron
- Boron TED was suppressed by those.



3D APT System

Y. Shimizu et al., APL, 98, 232101, 2011.



Summary

- ❒ Variation is the most important issue for the Advanced CMOS & LSI's.
- ❒ New variation evaluation method, Takeuchi plot, is very useful.
- ❒ Boron TED can be the origin of the larger Vth variation of NFET.
- ❒ To mitigate this variation of NFET, Carbon co-I/I technique is very useful.